

FIG.1 (PRIOR ART)

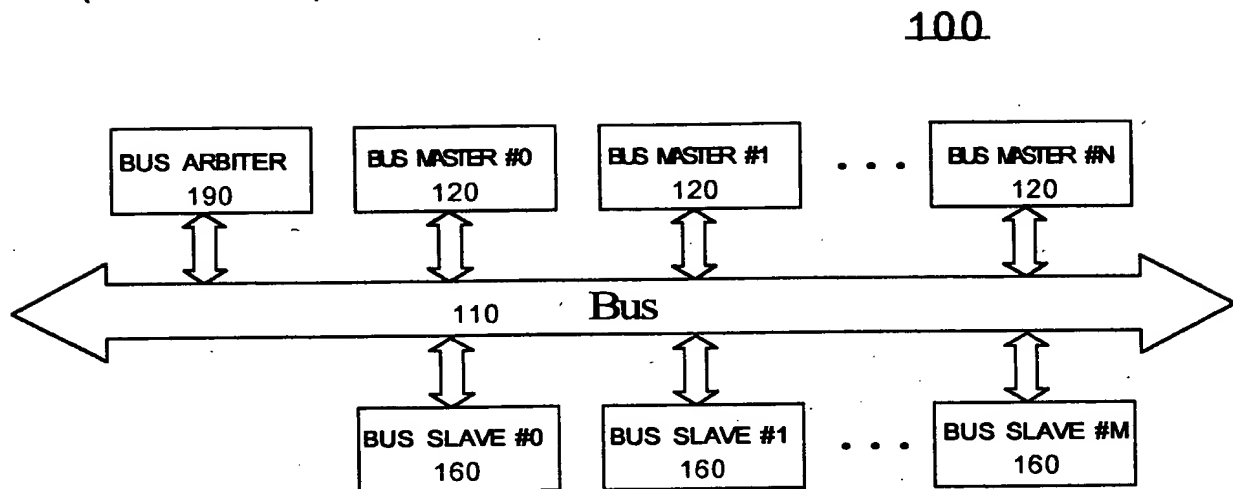
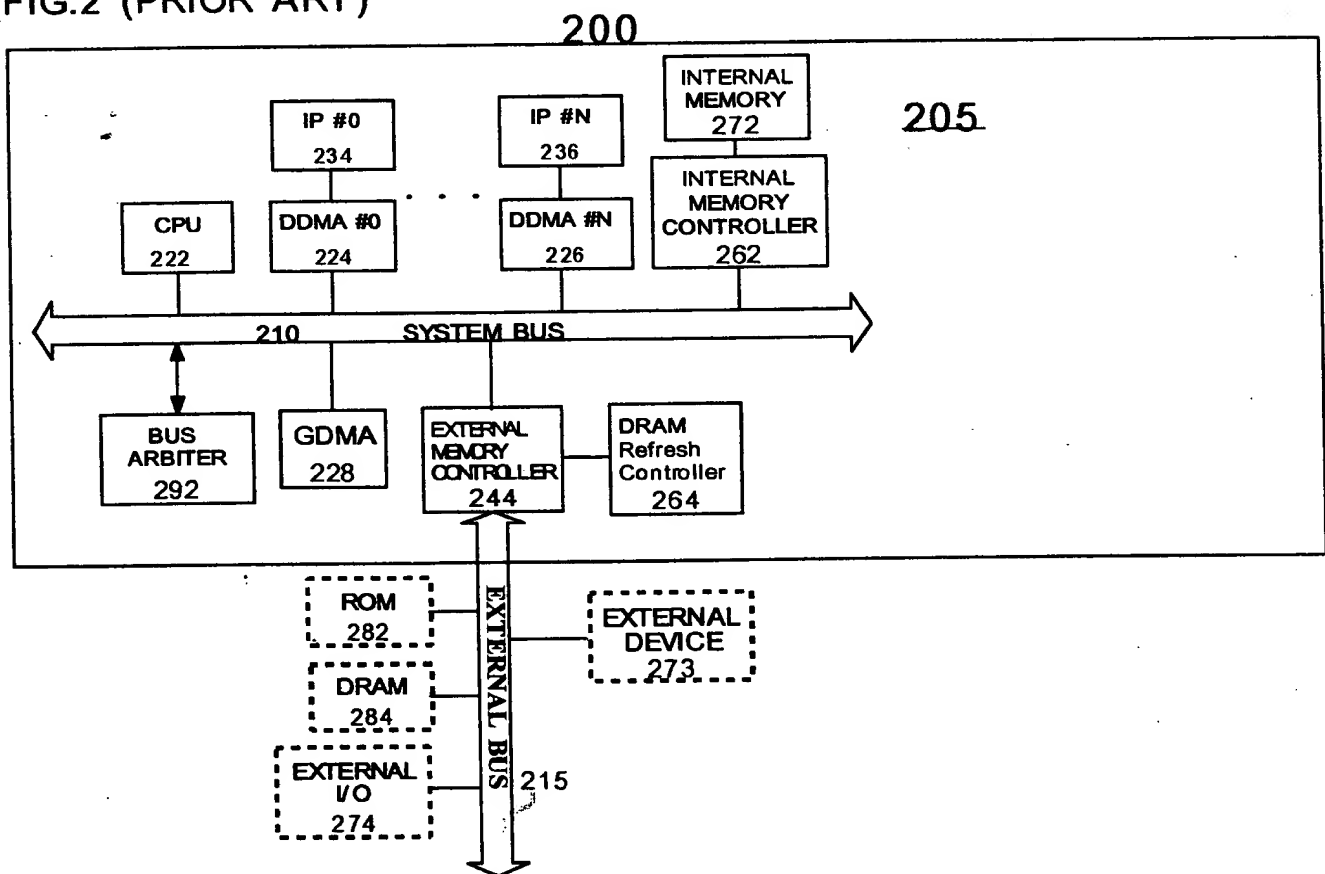


FIG.2 (PRIOR ART)



T01E10 128E2250

FIG.2B (PRIOR ART)

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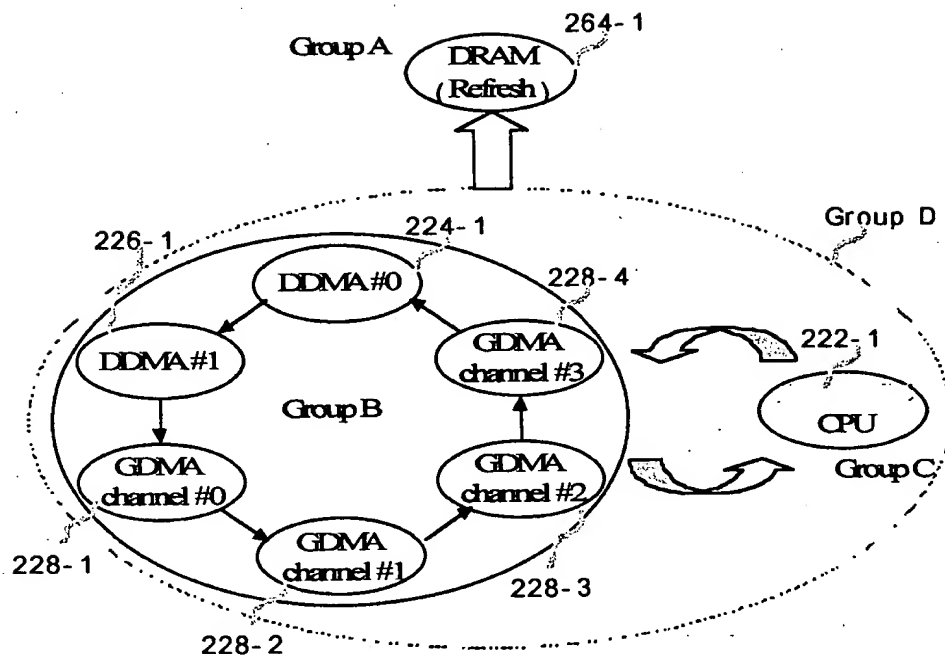


FIG.2C (PRIOR ART)

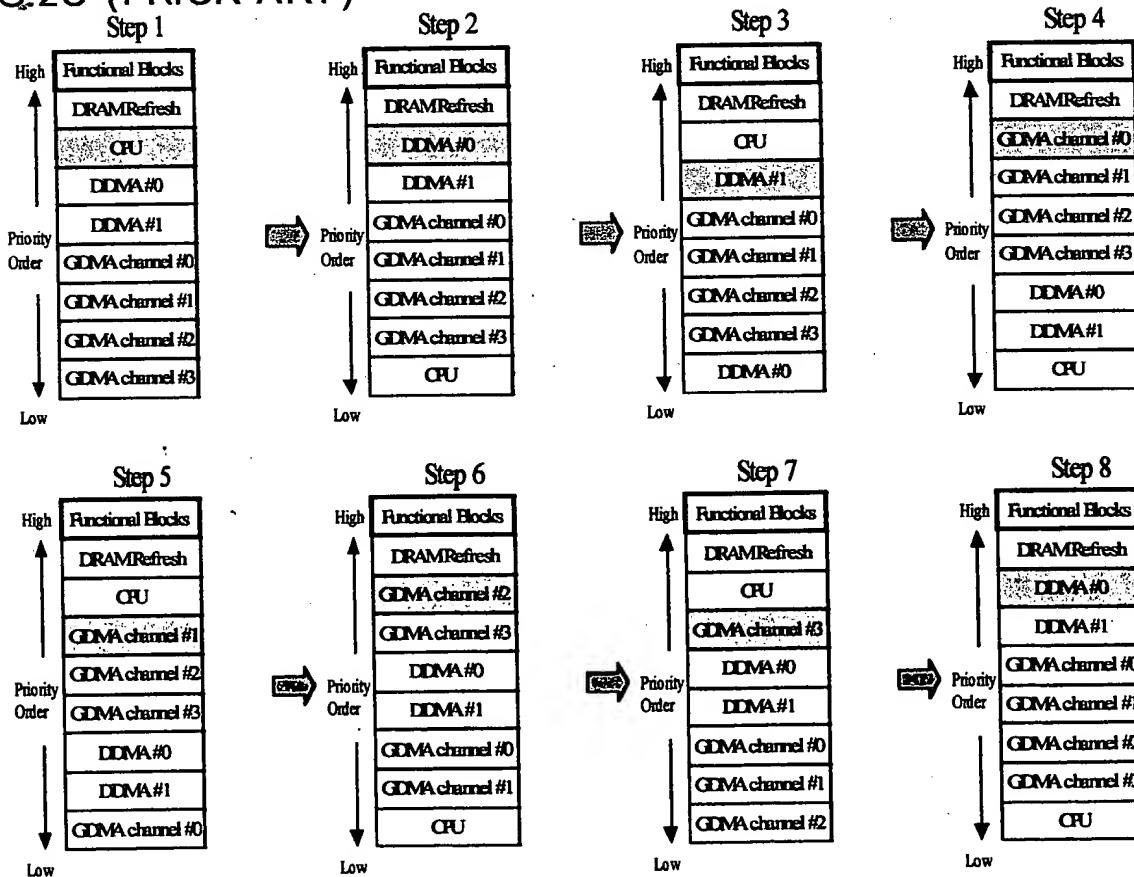
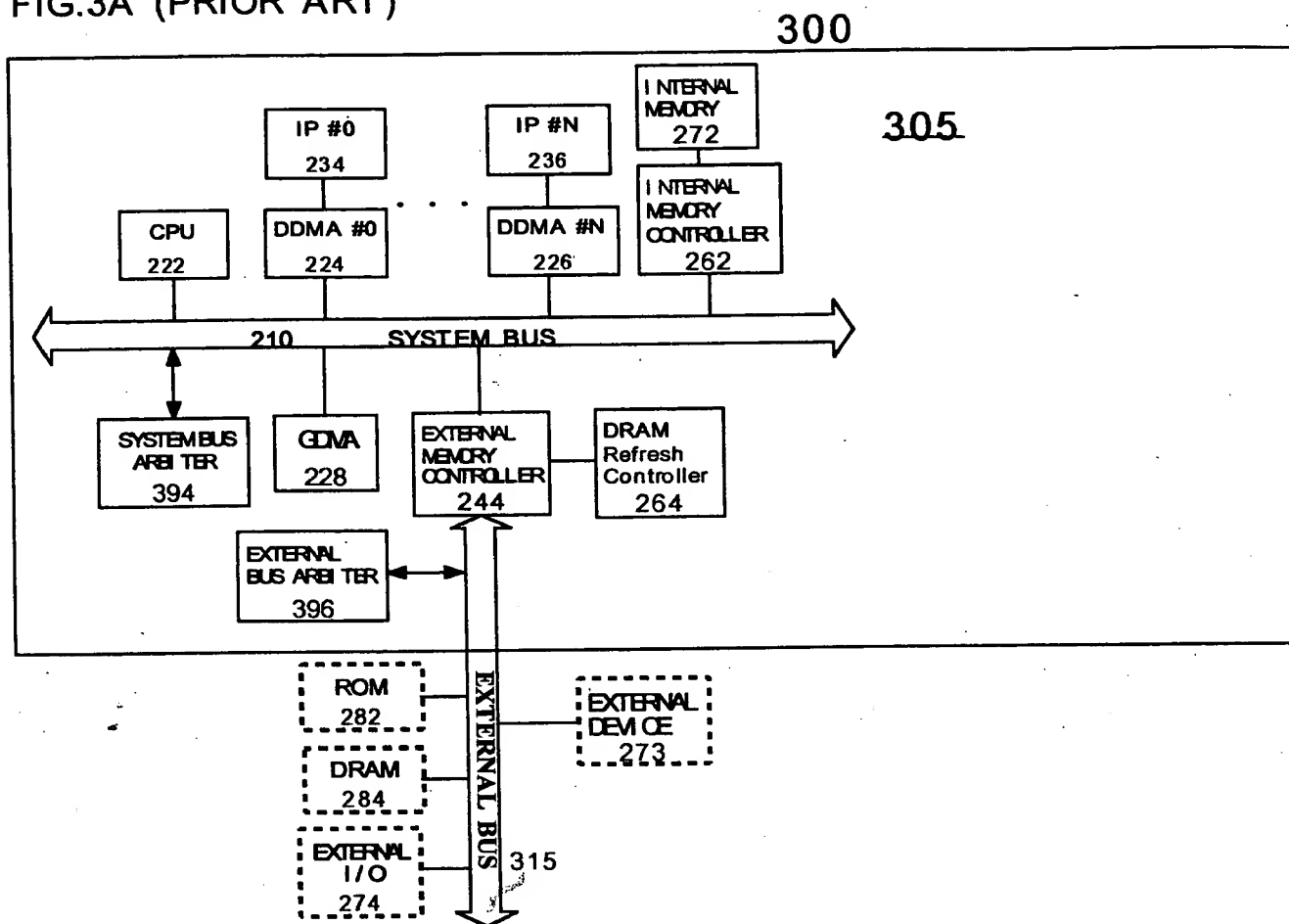


FIG.3A (PRIOR ART)



0973874, 011101

FIG.3B (PRIOR ART)

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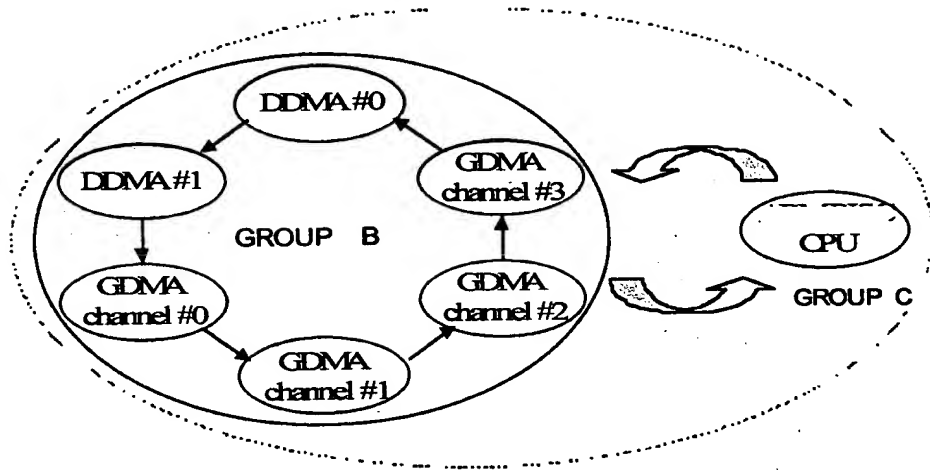


FIG.3C (PRIOR ART)

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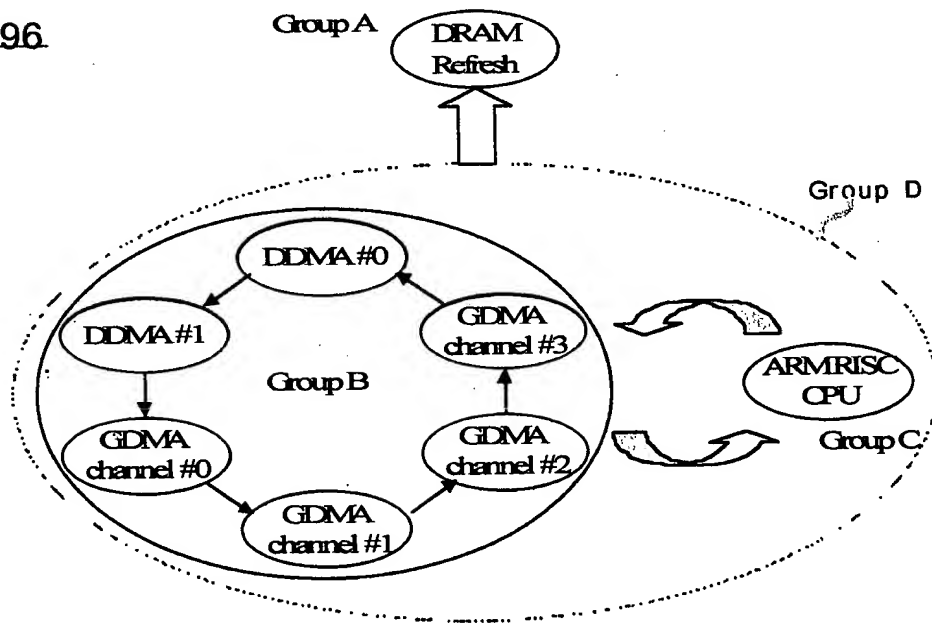


FIG.3D (PRIOR ART)

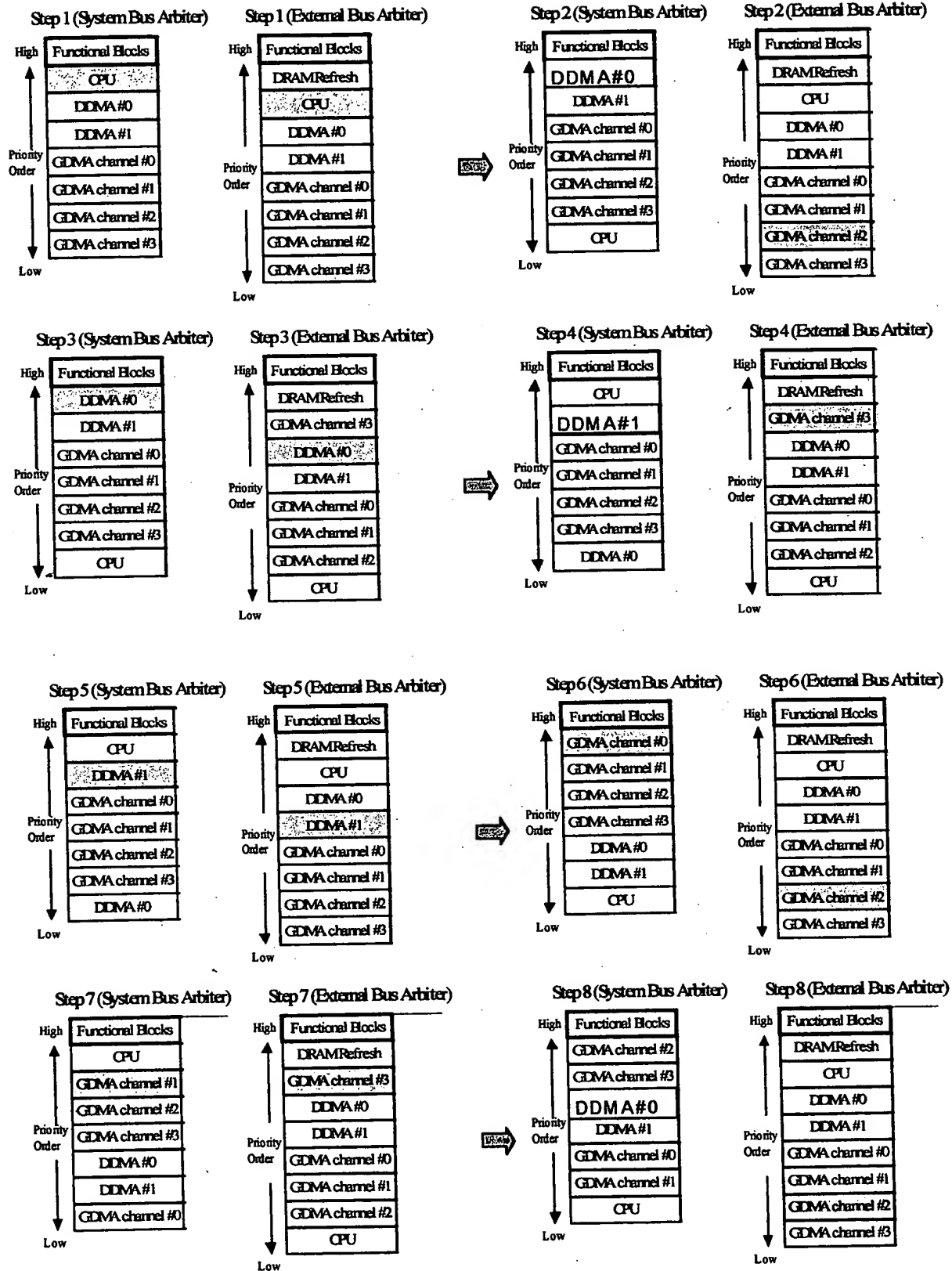
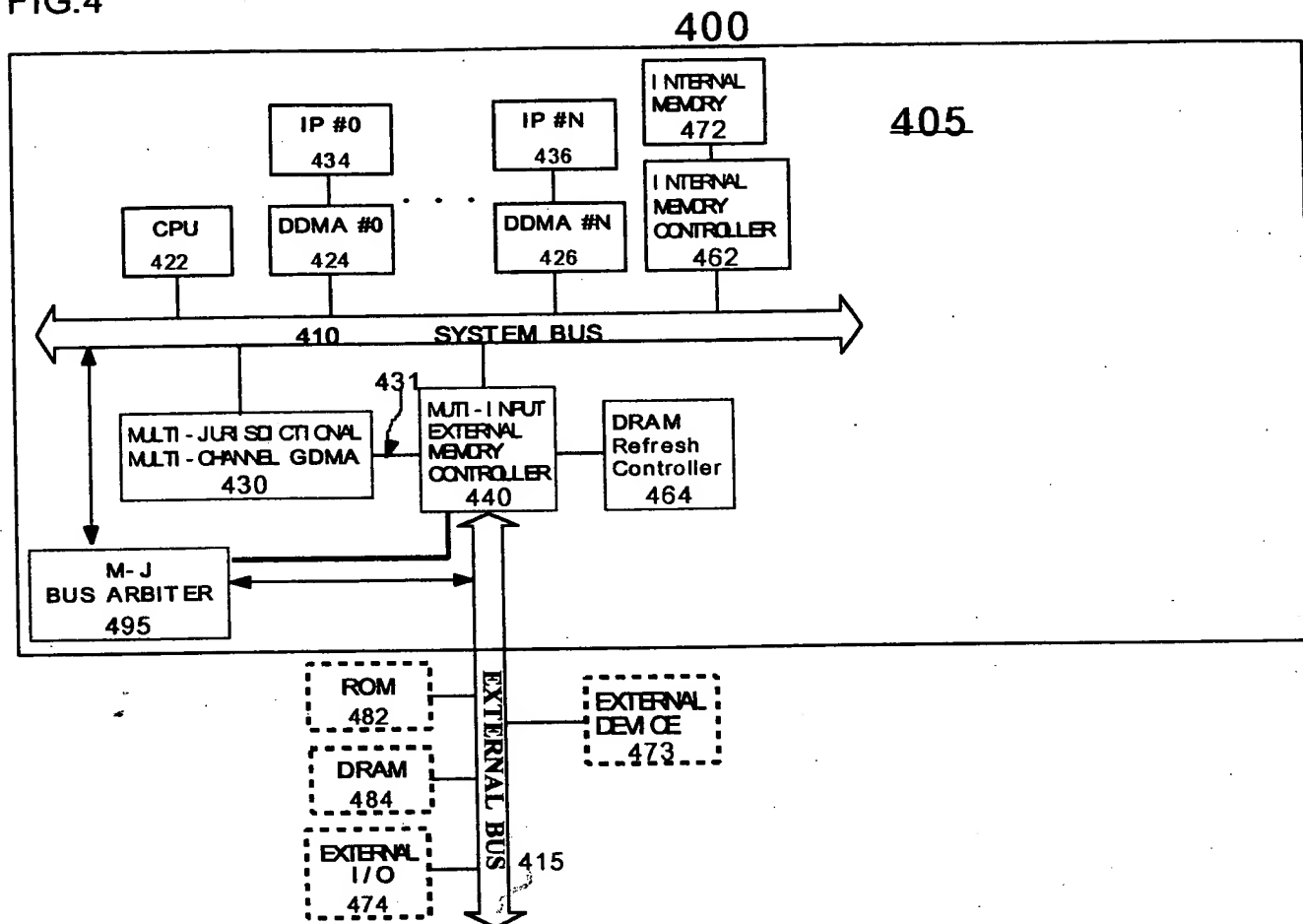
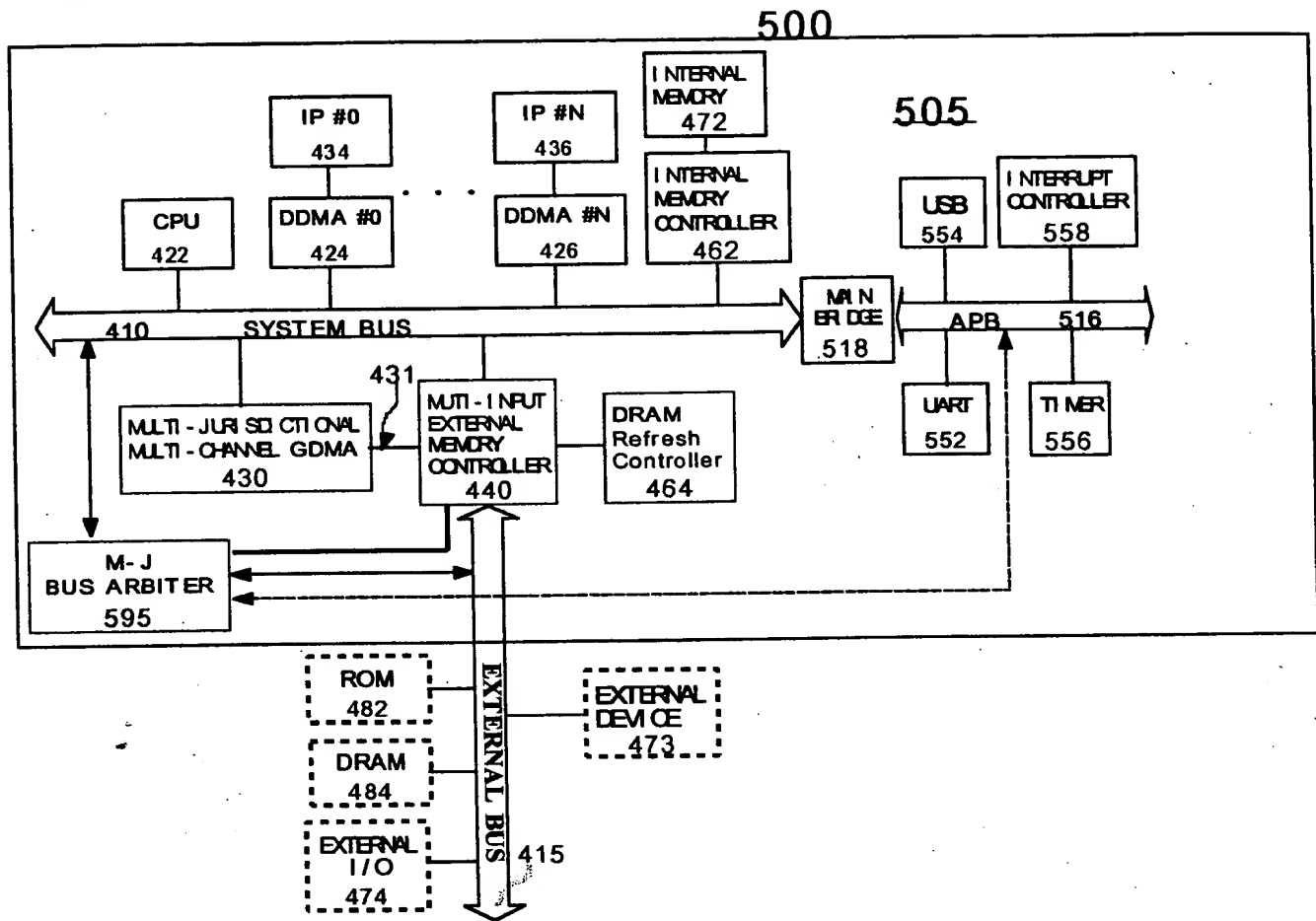


FIG.4



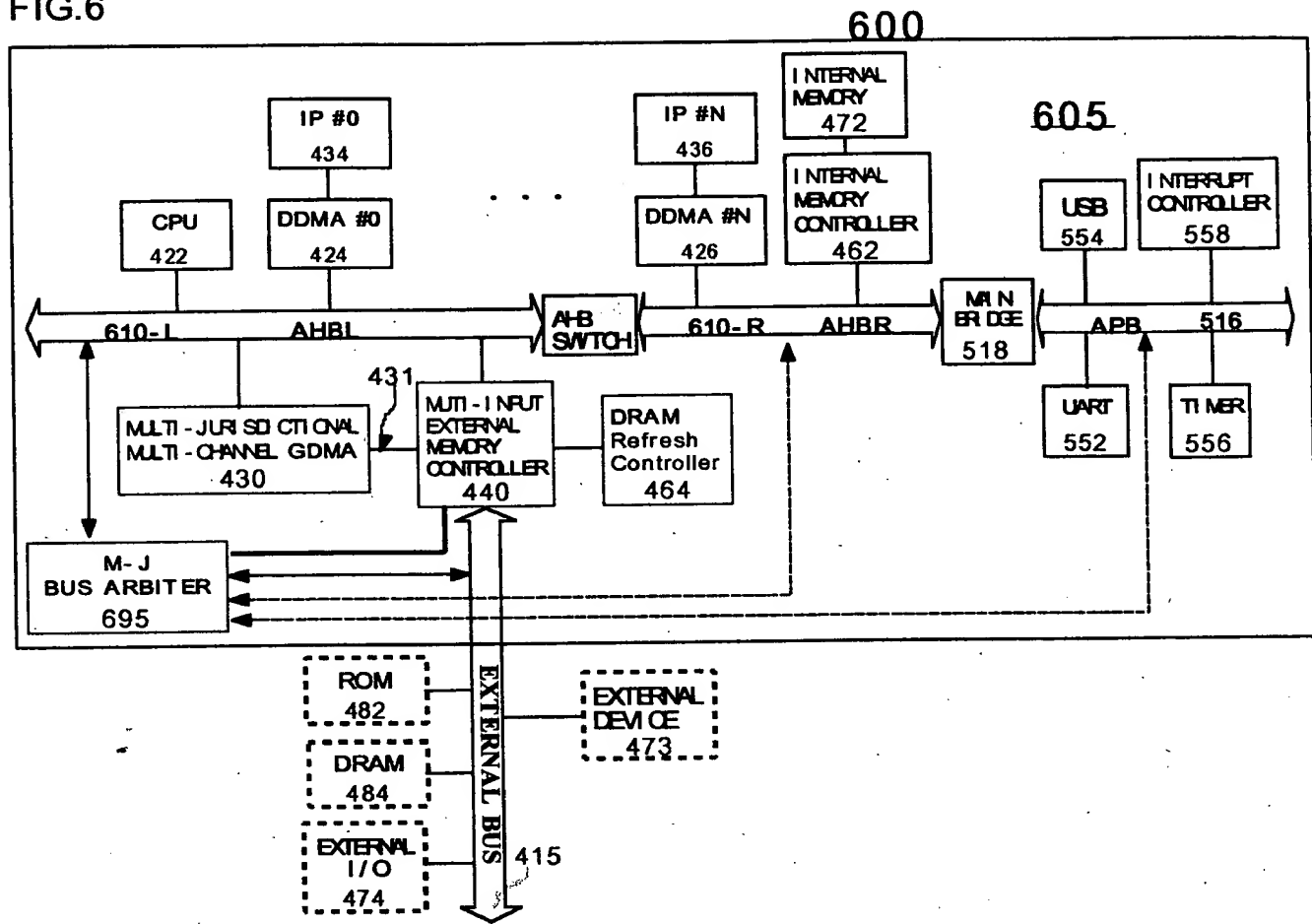
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FIG.5



0973674-01101

FIG.6



0973874-013101

FIG. 7

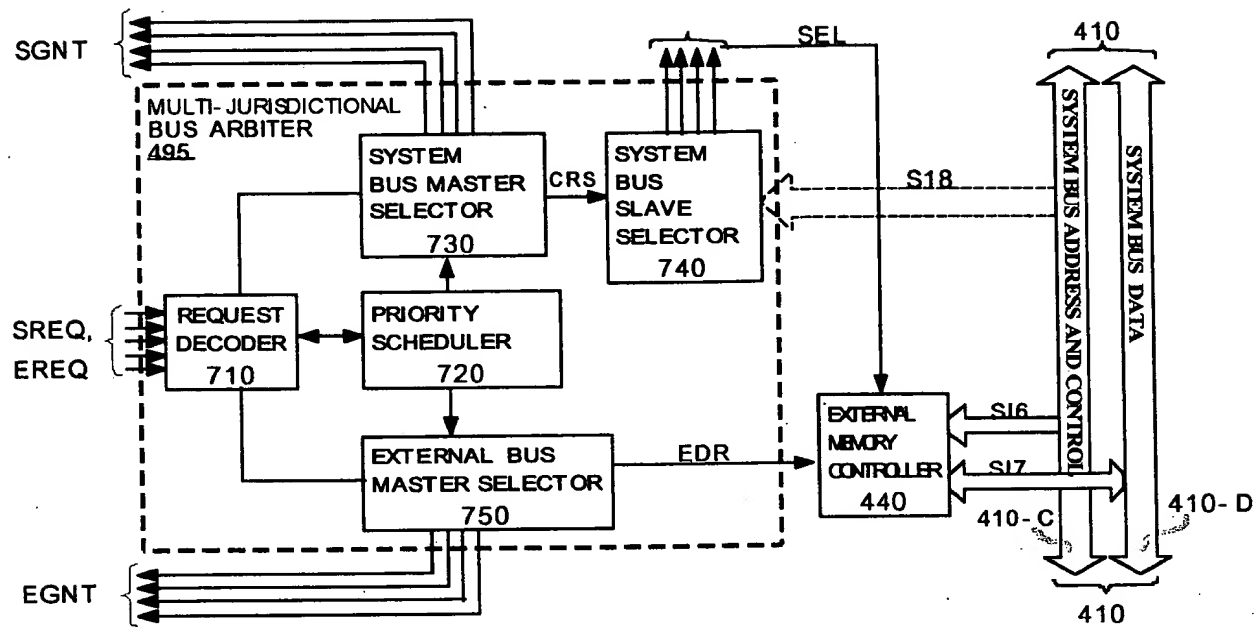


FIG. 7

FIG.8

TOP SECRET 423550

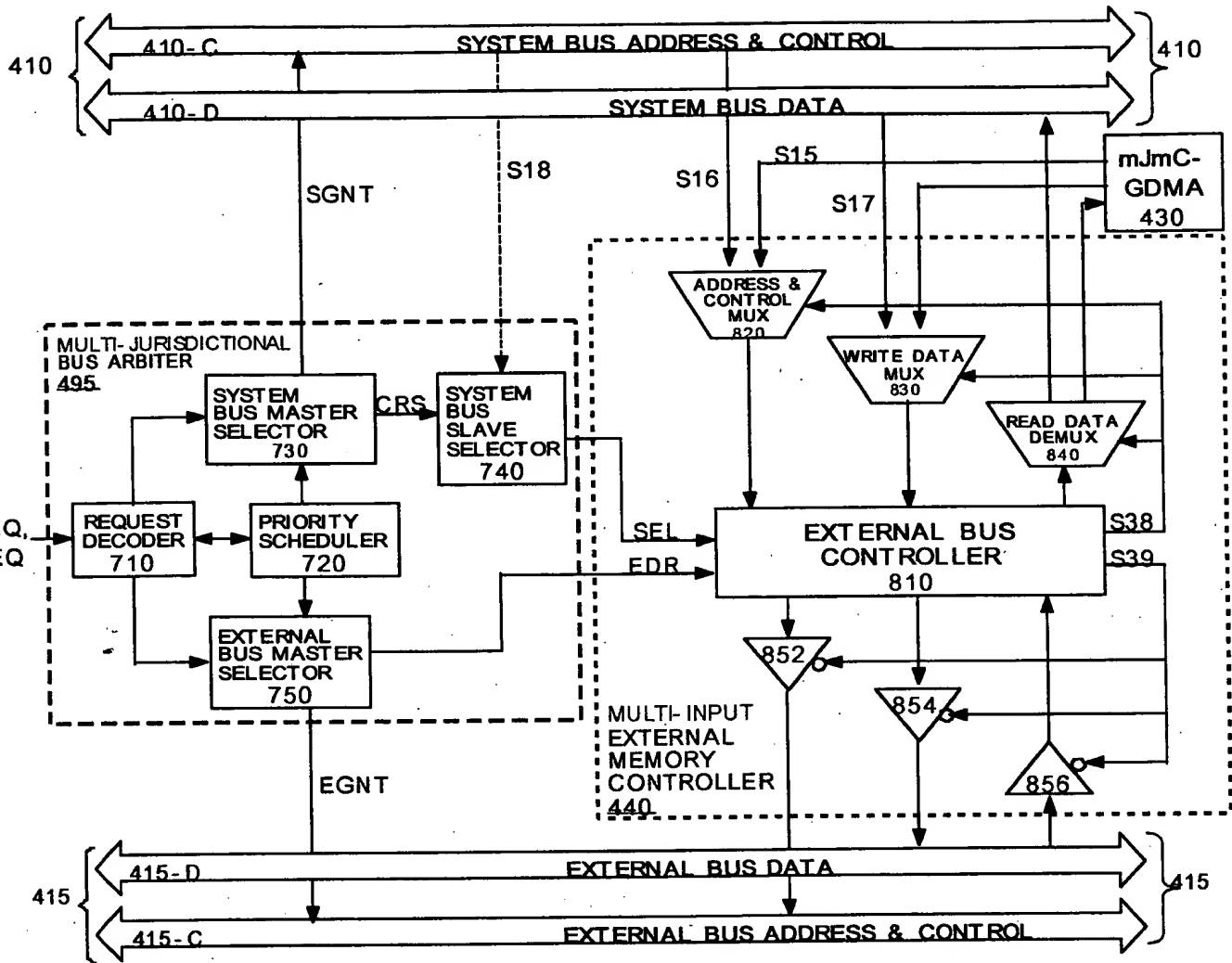


FIG.9

| | | External bus master | System bus master | |
|-------------------------|---------------------------------|--|--------------------------------------|---------------------------------|
| | No request REQ[1:0] = 2' b00 | External bus only REQ[1:0] = 2' b10 | System bus only REQ[1:0] = 2' b01 | Both buses REQ[1:0] = 2' b11 |
| DRAM refresh controller | O | O | X | X |
| CPU | O | X | O | O |
| DMA block | O | X | O | O |
| GMA channel | O | O | O | O |
| External device | O | O | X | X |

FIG.11

| Classification of set | Element |
|---|---|
| Set of functional blocks making a system bus request (system bus master, S) | CPU, DMA block, and GMA block |
| Set of functional blocks making an external bus request (E) | DRAM refresh controller, CPU, DMA block, GMA channel, and external device |
| Set of functional blocks making only a system bus request (SO) | CPU |
| Set of functional blocks making only an external bus request (EO) | DRAM refresh controller, GMA channel, and external device |
| Set of functional blocks making a request for both system bus and external bus (ES) | CPU, DMA block, and GMA channel |
| Set of functional blocks making requests for a system bus or an external bus (A) | DRAM refresh controller, CPU, DMA block, GMA channel, and external device |

FIG.10

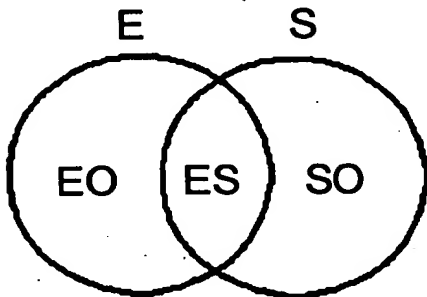


FIG.12

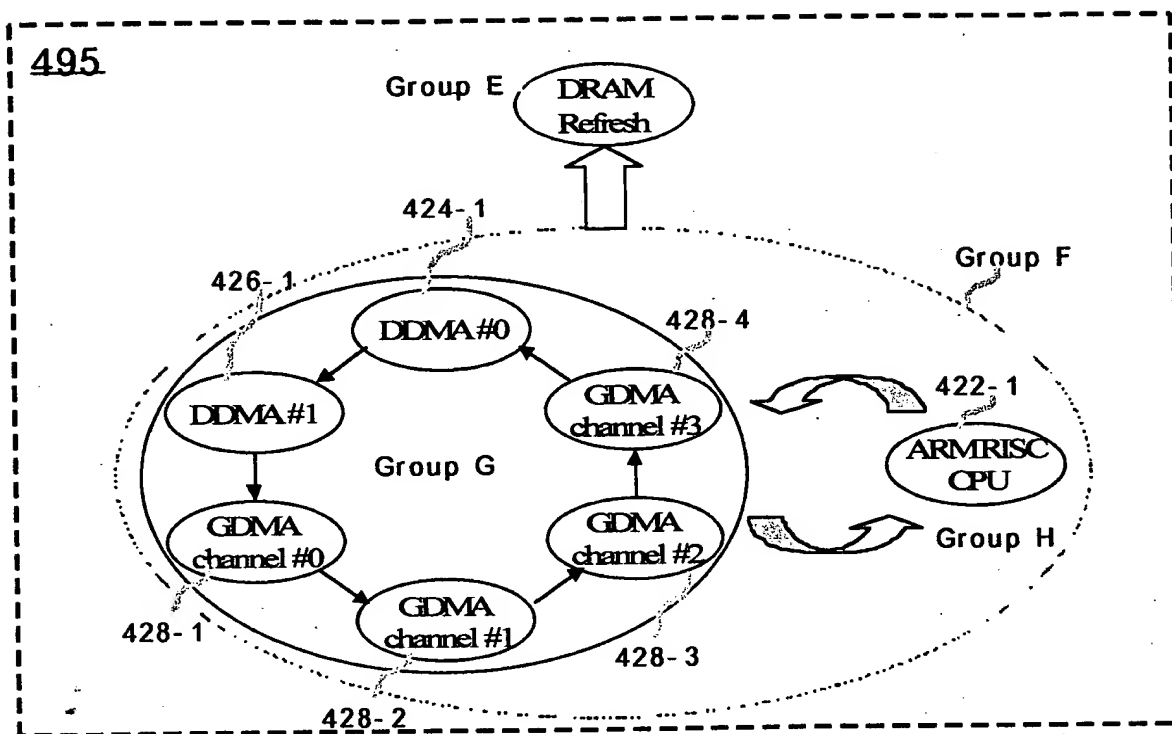
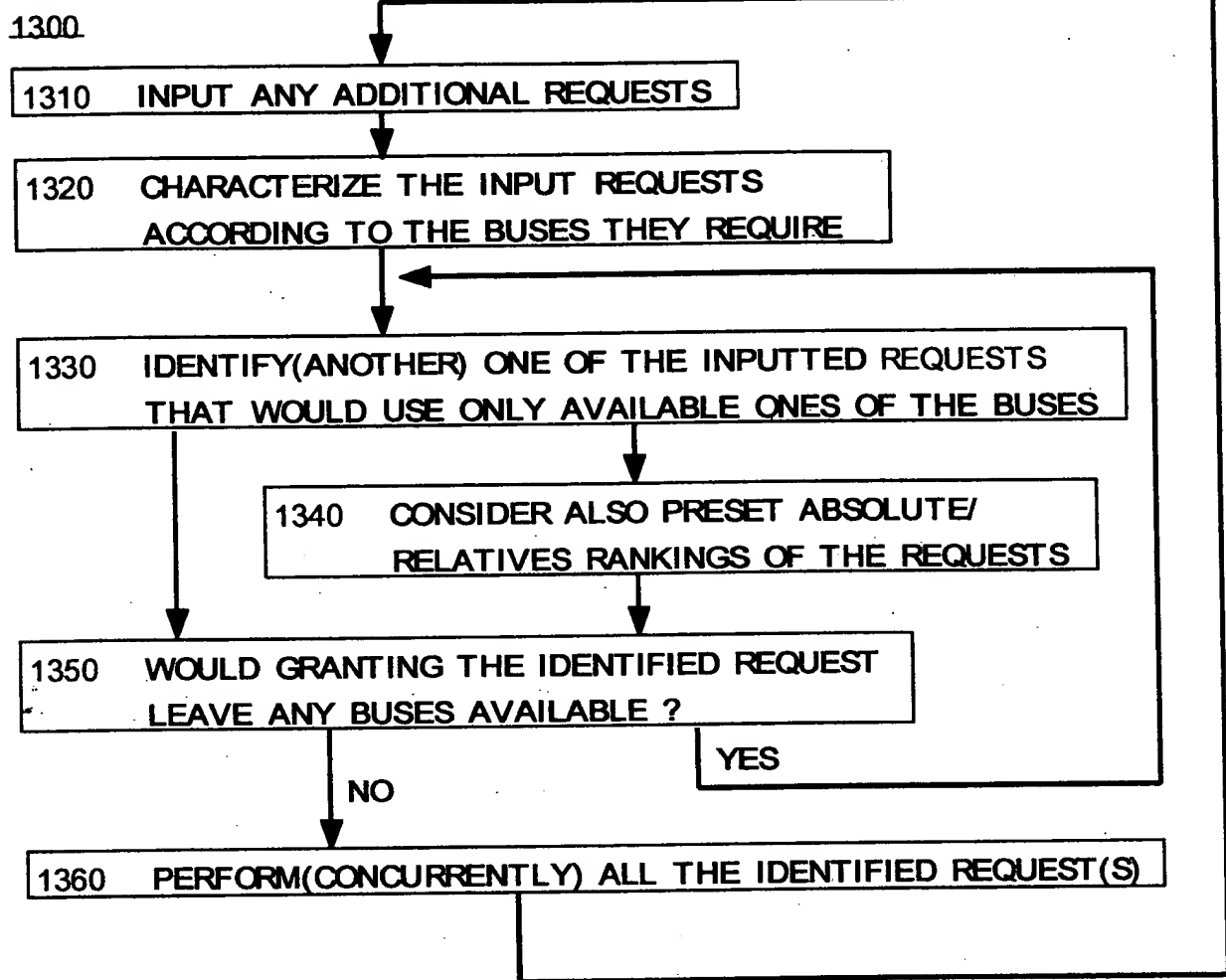


FIG.13



FORM 4322-250

FIG.14

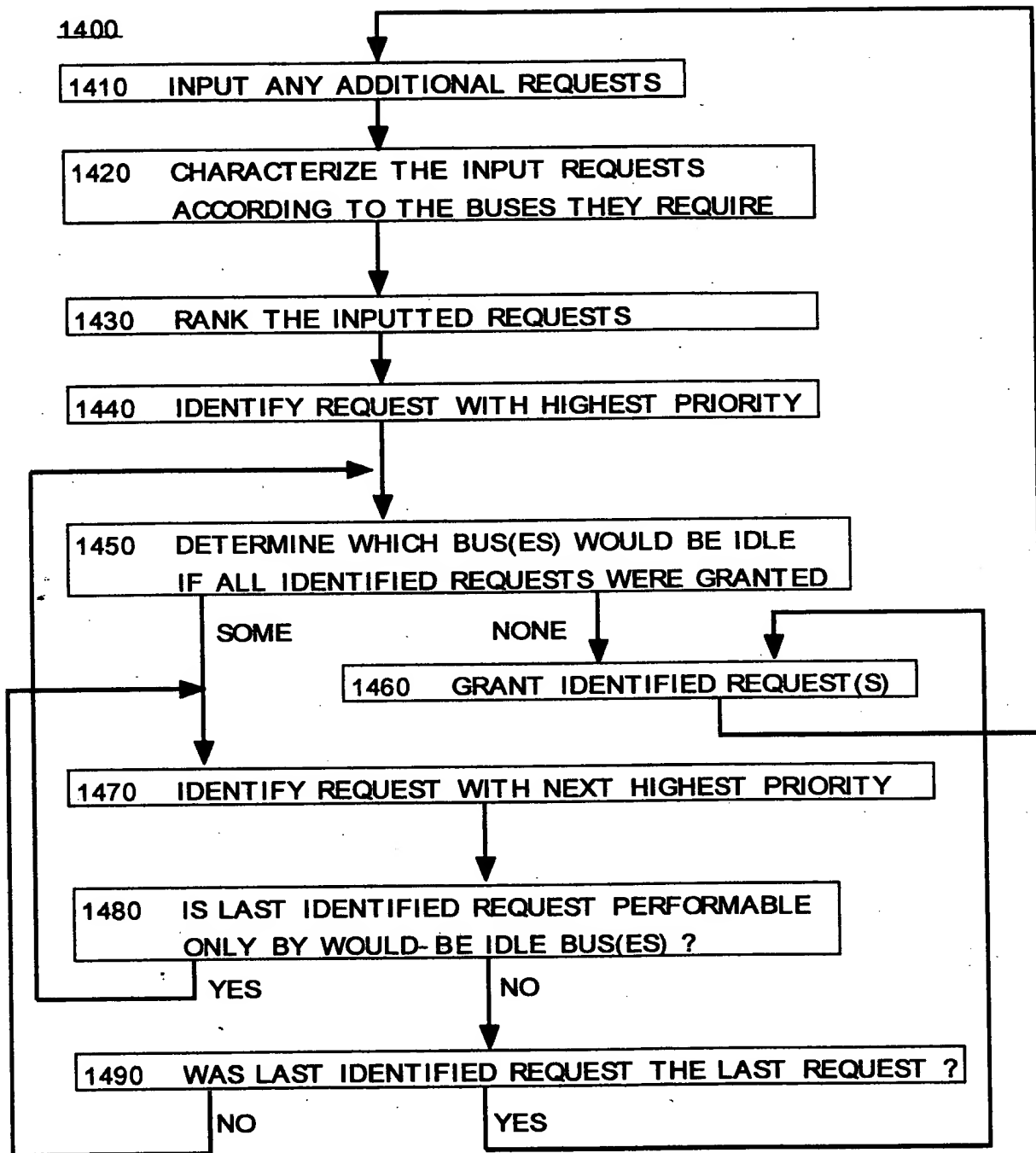


FIG. 14

FIG.15

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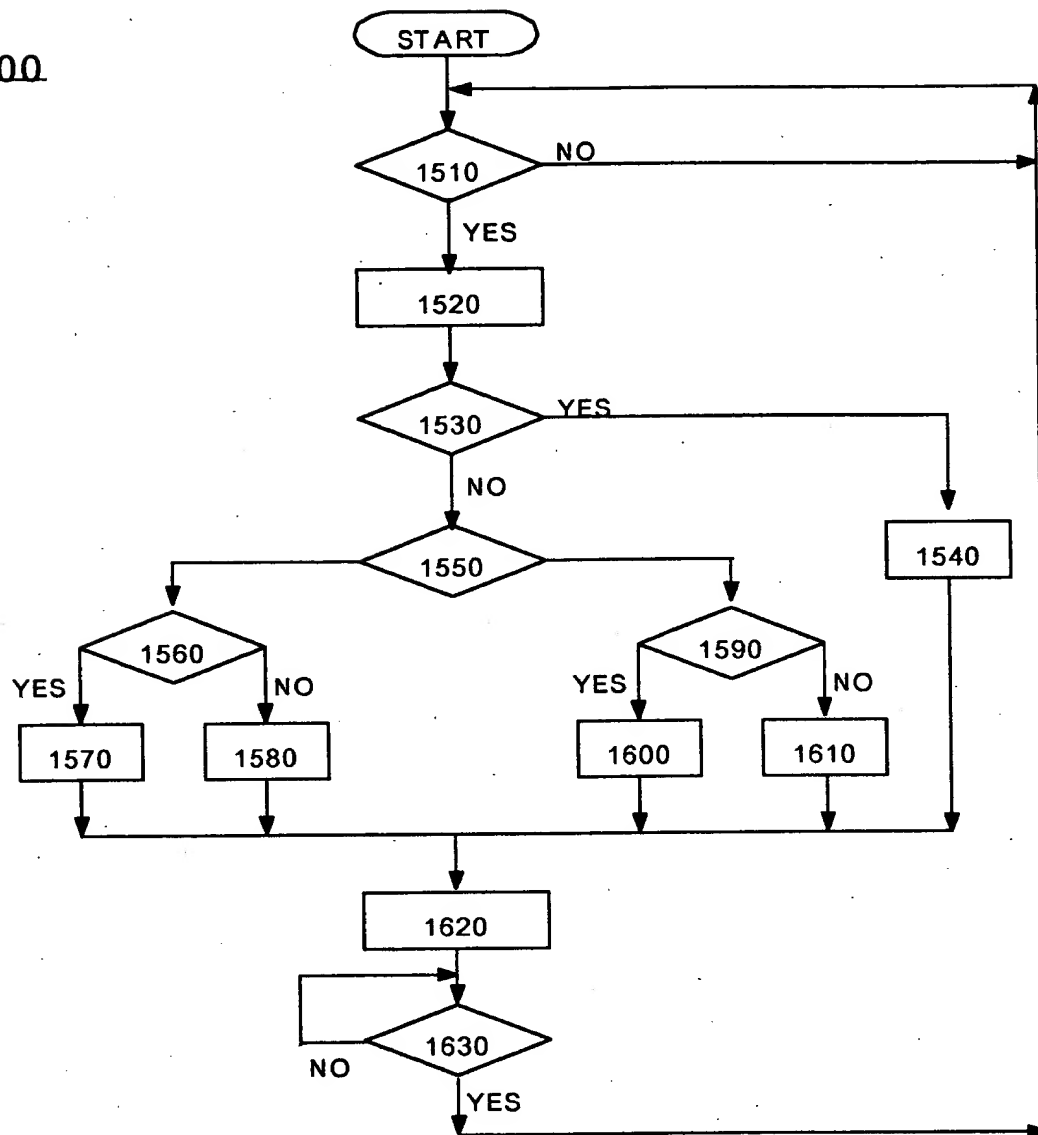


FIG.16

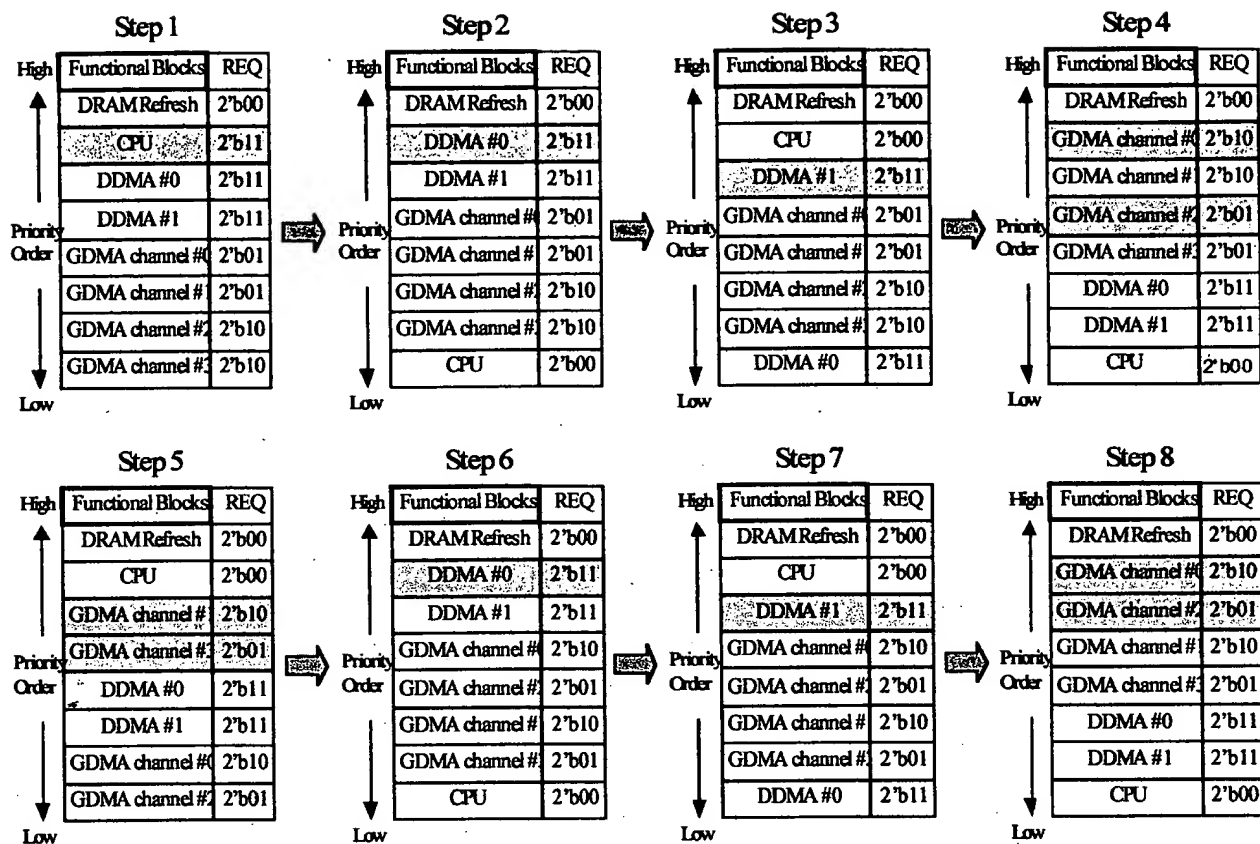


FIG.17

| Item | Probability that element having bus ownership performs operation | | | Bus utilization |
|------------------------------|--|-------------------|-----------------------------------|--|
| | Element of set EO | Element of set ES | Element of set SO | |
| Exclusive bus arbitration | $\frac{1}{n(A)}$ | $\frac{1}{n(A)}$ | $\frac{1}{n(A)}$ | $\frac{n(EO) + 2n(EO) + n(SO)}{2n(A)}$ |
| Hierarchical bus arbitration | $\frac{n(ES) + 2n(SO)}{2n(S)n(EO)}$ | $\frac{1}{2n(S)}$ | $\frac{1}{n(S)}$ | $\frac{4n(SO) + 3n(ES)}{4n(S)}$ |
| Present invention | $\frac{n(EO) + n(SO)}{n(A)n(EO)}$ | $\frac{1}{n(A)}$ | $\frac{n(EO) + n(SO)}{n(A)n(SO)}$ | 1 |